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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,205	03/16/2004	Warren M. Farnworth	2269-5774US (01-1281.00/U	3129

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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

NOTIFICATION DATE	DELIVERY MODE
04/09/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTOMail@traskbritt.com

Office Action Summary	Application No.	Applicant(s)	
	10/801,205	FARNWORTH ET AL.	
	Examiner	Art Unit	
	JUNGHWA M. IM	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *43-84* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *43-84* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/31/2007 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 43-44, 46, 49-53, 55, 64-65, 68-72 and 75 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (US 6768190), hereinafter Yang in view of Takata et al. (US 20020027279), hereinafter Takata.

Regarding claims 43, 44 and 64, Fig. 2 of Yang shows a method of forming a semiconductor die (120) connected to at least one component and a substrate (110) comprising:

providing a semiconductor die having an active surface (122) and an inactive surface (123), the semiconductor die including at least one bond pad (bond pad on the

right) formed on a portion of the active surface connected to the at least one circuit and an area of metal (bond pad in the middle) on the semiconductor die free of connection to a circuit of the semiconductor die or another semiconductor die;

and at least one bond pad formed on a portion of the inactive surface; and

attaching the substrate (110) having a portion thereof connected to the at least one bond pad formed on the portion of the active surface of the semiconductor die by applying a force.

Yang shows most aspects of the instant invention except performing on a semiconductor die to lower stress of a portion of the semiconductor die to protect a portion of the semiconductor die, land lowering stress of a portion of the semiconductor die by placing the at least one bond pad on a portion of the inactive surface of the semiconductor die distributing the forces therearound, and protecting a portion of the semiconductor die from stress on the semiconductor die by circuits located on the active surface of the semiconductor die. Fig. 4 of Takata shows a bond pad (17a, 17c) on the surface of the semiconductor device to reduce the stress in the semiconductor device. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Takata into the device of Yang in order to have at least one bond pad on a portion of the inactive surface of the semiconductor die for distribution of the forces therearound and protection of the semiconductor die to improve the reliability of the device.

Regarding claim 46, Fig. 2 of Yang shows that the area of metal comprises at least one bond pad formed on a portion of an inactive surface of the semiconductor die connected to a circuit of the semiconductor die.

Regarding claims 49 and 68, Fig. 2 of Yang shows that forming the substrate having a portion thereof connected to the at least one bond pad formed on a portion of the inactive surface of the semiconductor die, the substrate having at least one circuit connected to the at least one bond pad of the semiconductor die; and at least one bond wire (160) connected to the at least one bond pad formed on the inactive surface of the semiconductor die.

Regarding claim 50, Fig. 2 of Yang shows that the substrate includes a portion thereof located adjacent at least one edge of the semiconductor die.

Regarding claims 51 and 70, Fig. 2 of Yang shows applying a sealant material (170) located between a portion of the semiconductor die and a portion of the substrate.

Regarding claims 52 and 71, Fig. 2 of Yang shows applying a sealant material (170) located along a portion of at least one edge of the semiconductor die and a portion of the substrate.

Regarding claim 53, Fig. 2 of Yang shows at least one bond pad formed on the inactive surface to a contact pad on a portion of a surface of the substrate.

Regarding claims 55 and 75, the combination of Yang/Takata fails to show the at least one bond pad formed on the inactive surface of the semiconductor die includes a shape of one of a square shape, rectangular shape, circular shape, elliptical shape, hexagonal shape, and triangular shape. However, it would have been obvious matter of

accommodating required specification since such a modification would have involved a mere change in the shape of a component. A change in shape is generally recognized as being within the level of ordinary skill in the art. *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Regarding claim 65, Fig. 2 of Yang shows the at least one bond pad formed on the portion of the inactive surface of the semiconductor die includes a bond pad connected to a circuit of the semiconductor die.

Regarding claim 69, Fig. 2 of Yang shows the substrate includes a portion thereof located adjacent at least one edge of the semiconductor die.

Regarding claim 72, Fig. 2 of Yang shows connecting the at least one bond pad formed on the portion of the active surface of the semiconductor die to a contact pad on a portion of a surface of the substrate.

Claims 47-48, 62-63, 66-67 and 83-84 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang and Takata as applied to claims 43 and 64 above, and further in view of Chu et al. (US 20040099961), hereinafter Chu.

Regarding claims 47 and 66, the combination of Yang/Takata fails to show "wherein the at least one bond pad formed on a portion of the inactive surface includes a bond pad having more than one layer of material." Fig. 6B of Chu discloses a bond pad (35) having more than one layer of material (35c, para [0032]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include bond pads of more than one layer in the device of Yang/Takata in order to improve the affinity of the bond pads to the device.

Regarding claims 48 and 67, Chu discloses a bond pad having more than one layer of material, each layer of material comprising a different metal (para [0032]). In addition, it is inherent that the different metal materials, specifically copper and gold, have different coefficients of thermal expansion.

Regarding claims 62 and 83, the combination of Yang/Takata does not explicitly show "wherein the semiconductor die includes at least one trace extending from at least a portion of the area of metal formed on the surface of the semiconductor die." However, it is obvious that a trace extends from at least a portion of the area of metal formed on the portion of the active surface of the semiconductor die since such a trace is necessary to operate the signal terminals of the device.

Regarding claims 63 and 84, the combination of Yang/Takata does not explicitly show "one connector located on a portion of the at least one trace." However, it is obvious that at least one connector is located on a portion of the at least one trace since such a trace is necessary to operate the signal terminals of the device.

Claims 54, 56-57, 61, 73-74, 76 and 78 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang and Takata as applied to claims 43, 49, 64, 66 and 68 above, and further in view of Doan (US 20050167798).

Regarding claims 54 and 77, the combination of Yang/Takata fails to show "a method further comprising: attaching at least one resilient connector to a portion of the active surface of the semiconductor die and a portion of a surface of the substrate." Doan discloses a method (para [0040]) further comprising: attaching at least one resilient connector (148 in Fig. 3A) to a portion of the active surface (144) of the semiconductor die and a portion of a surface of the substrate (para [0015]).

It would have been obvious to one of ordinary skill in the art to attach resilient connectors in the device of Yang/Takata to improve the reliability of the device package.

Regarding claims 56 and 73-74, Doan discloses a method (para [0040]) wherein the substrate (para [0015]) includes at least one resilient connector (148, para [0039]) located on a surface thereon abutting a portion of the semiconductor die.

Regarding claims 57, 61 and 78, the combination of Yang/Takata fails to show "the semiconductor die includes at least a portion of one metal protection layer located on a portion of an active surface thereof." Fig. 3B of Doan shows a method (para [0040]) wherein the semiconductor die includes at least a portion of one metal protection layer (146) located on a portion of an active surface (144) thereof.

It would have been obvious to one of ordinary skill in the art to incorporate the teachings of Doan in the device of Yang/Takata in order to have to a portion of one metal protection layer located on a portion of an active surface to protect the device package.

Regarding claim 76, the combination of Yang/Takata/Doan fails to show the at least one bond pad formed on the inactive surface of the semiconductor die includes a

shape of one of a square shape, rectangular shape, circular shape, elliptical shape, hexagonal shape, and triangular shape. However, it would have been obvious matter of accommodating required specification since such a modification would have involved a mere change in the shape of a component. A change in shape is generally recognized as being within the level of ordinary skill in the art. *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Claims 45, 58-60 and 79-82 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang and Takata as applied to claims 43 and 64 above, and further in view of Kuo et al. (US 20050121804), hereinafter Kuo.

Regarding claims 45, 58 and 79, the combination of Yang/Takata fails to show the semiconductor die includes a passivation layer or a first passivation layer located on a portion thereof and a second passivation layer located on a portion of the first passivation layer. Fig. 1F of Kuo shows a semiconductor die which includes a first passivation layer (192c) located on a portion thereof and a second passivation layer (192d) located on a portion of the first passivation layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the Kuo's teaching to include a second passivation layer located on a portion of a first passivation layer located on a die in the device of Yang/Takata to protect the device.

Regarding claims 59 and 80, the combination of Yang/Takata fails to show "a first passivation layer located on a portion of the one metal protection layer, and a second

passivation layer located on a portion of the first passivation layer." Fig. 1F of Kuo discloses a semiconductor die (100) which includes a first passivation (192c) layer located on a portion of the one metal protection layer (150b, para [0028]), and a plurality of passivation layers (para [0033]) located on a portion of the first passivation layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a plurality of passivation layers located on a portion of a first passivation layer located on a metal protection layer located on a die in the invention of Yang/Takata for protection of the device

Regarding claims 60 and 81-82, the combination of Yang/Takata fails to show "wherein the semiconductor die includes at least a portion of more than one metal protection layer located on a portion of an active surface thereof, a first passivation layer located on a portion of the more than one metal protection layer, and a plurality of passivation layers located on at least a portion of the first passivation layer." Fig. 1F of Kuo discloses semiconductor die (100) includes at least a portion of more than one metal protection layer (150a, 150b, para [0028], para [0033]) located on a portion of the active surface of the semiconductor die, a first passivation layer located on a portion on the metal protection layer, and a plurality of passivation layers (para [0033]) located on at least a portion of the first passivation layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include more than one metal protection layer located on a portion of the active surface of the semiconductor die in the invention of Yang/Takata for better adhesion of the metal layer.

Response to Arguments

Applicant's arguments filed August 9, 2007 have been fully considered but they are not persuasive. The rejection stands, modified only to accommodate the amendments made to the claims by Applicant. New rejections are made in response to Applicant amended claims. In addition, the examiner presents the remarks below in response to Applicant's arguments.

Applicants argue in length that "There in no teaching or suggestion that the electrode pads 17a and 17c either relieve stress or protect the upper surface of the semiconductor chip 11 whatsoever in the Takata et al. reference. ... Nowhere in the Takata et al. reference is there any discussion of the use of a varying bond pad pattern reducing the bending moment of the combination of a semiconductor chip, lead frame, and encapsulation material when the encapsulated semiconductor chip and lead frame are removed from the mold cavity. ..." Note that the center electrodes (17c) are distributed electrodes and a parallel arragement with other electrodes makes it possible to form a semiconductor package having a high rigidity (paragraph [0072]). Therefore, the combination of the Yang/Takata et at. reference does teach or suggest the claim limitations of the claimed inventions of independent claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JUNGHWA M. IM whose telephone number is (571)272-1655. The examiner can normally be reached on MON.-FRI. 7:30AM-4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Junghwa M. Im/
Examiner, Art Unit 2811

/J. M. I./